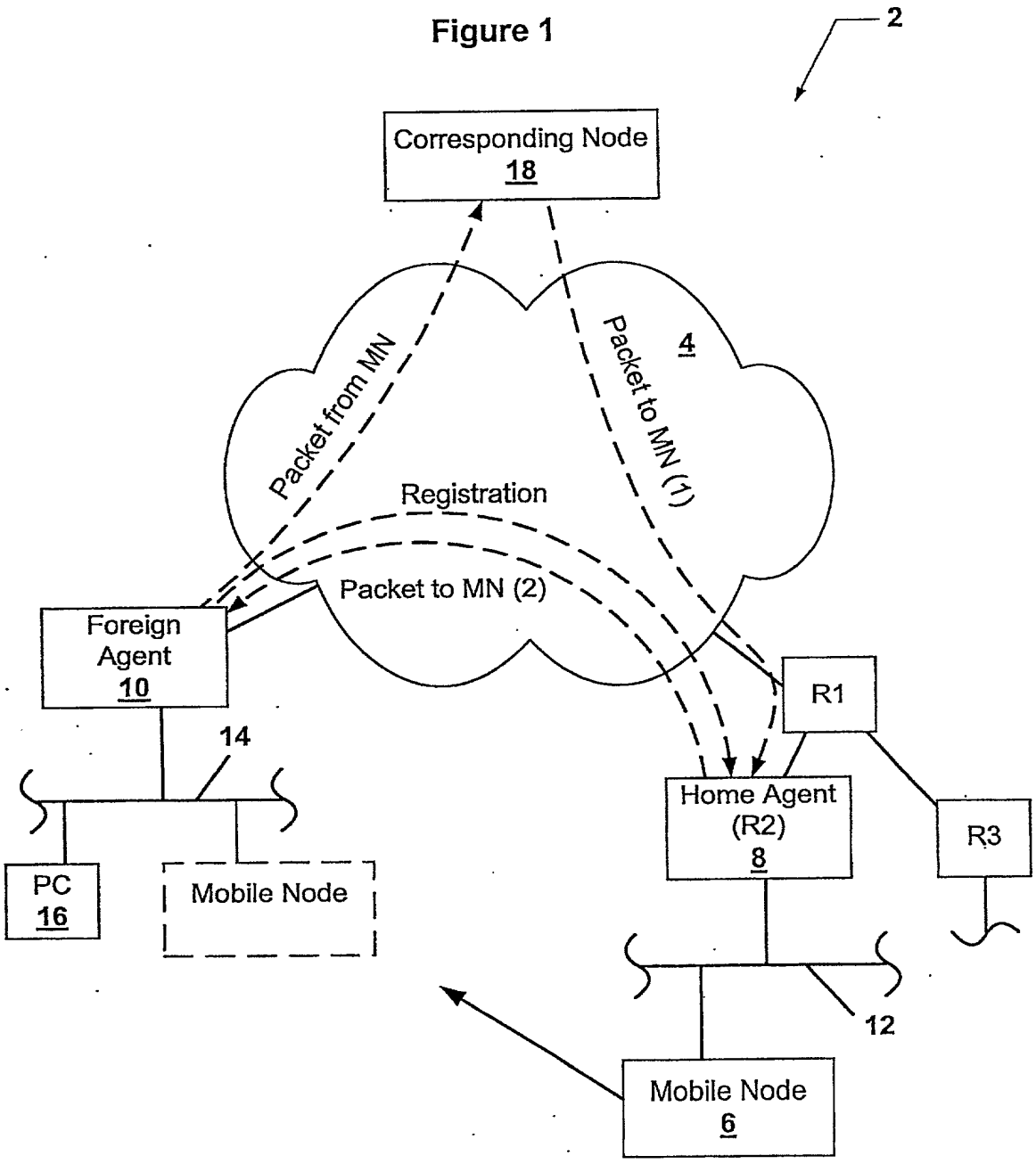
Figure 1


2
Corresponding Node
18
4
Packet from MN
Packet to MN (1)
Registration
Packet to MN (2)
Foreign
Agent
10
R1
14
Home Agent
(R2)
8
R3
PC
16
Mobile Node
12
Mobile Node
6

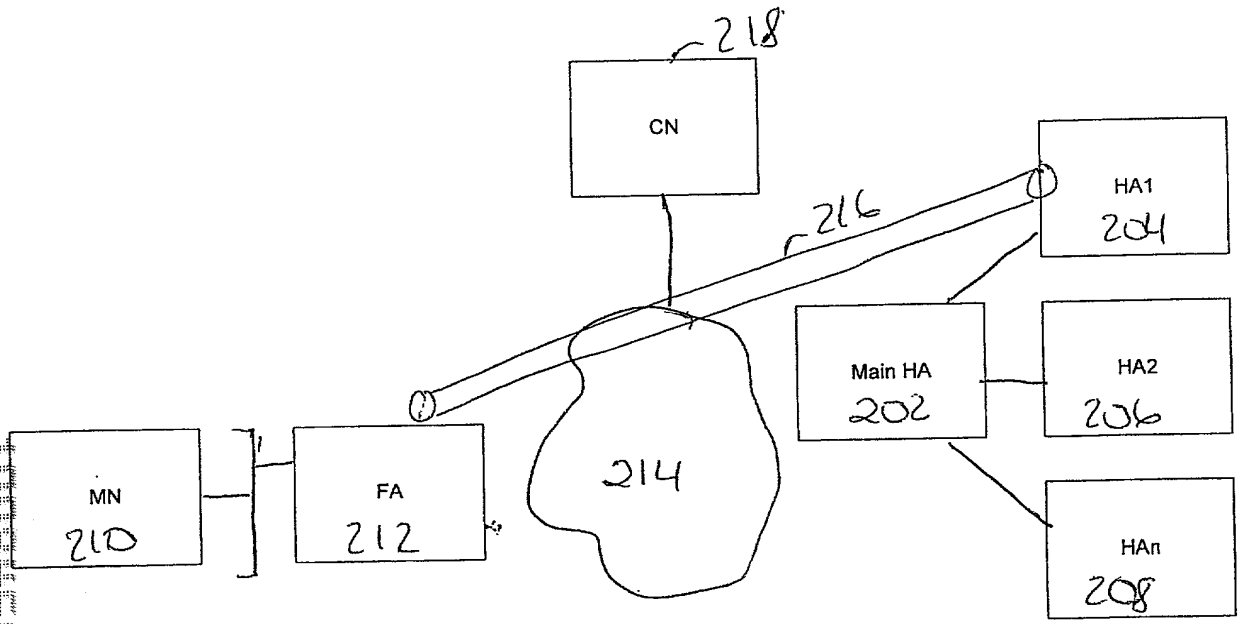


FIG. 2

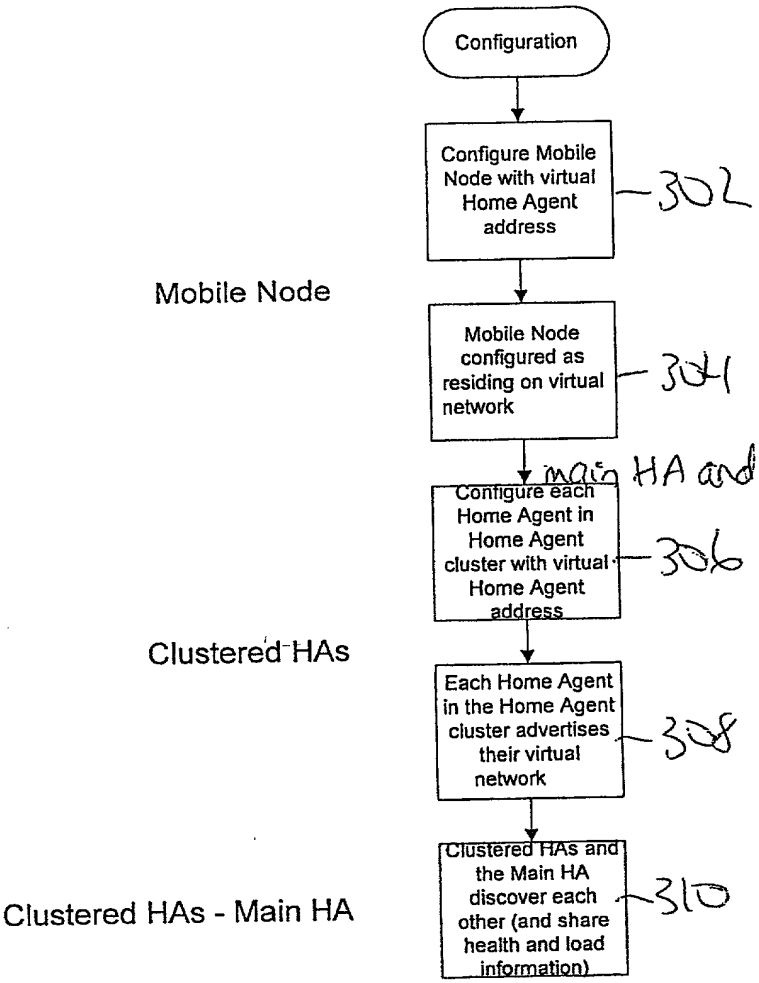

Configuration
Configure Mobile Node with virtual Home Agent address
302
Mobile Node
Mobile Node configured as residing on virtual network
304
main HA and
Configure each Home Agent in Home Agent cluster with virtual Home Agent address
306
Clustered HAs
Each Home Agent in the Home Agent cluster advertises their virtual network
308
Clustered HAs and the Main HA discover each other (and share health and load information)
310
Clustered HAs - Main HA

FIG. 3

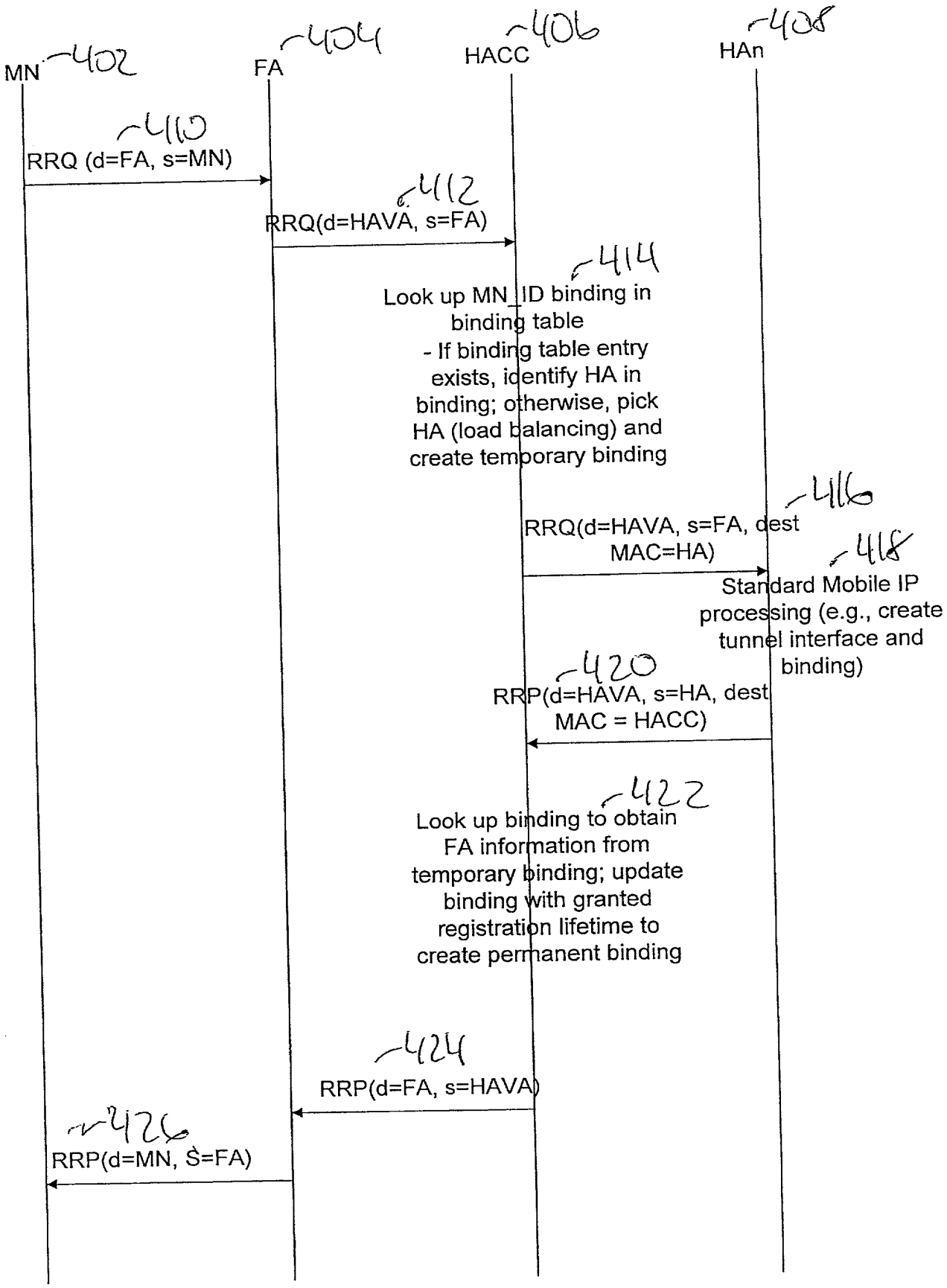

MN
402
FA
404
HACC
406
HAn
408
410
RRQ (d=FA, s=MN)
412
RRQ(d=HAVA, s=FA)
414
Look up MN_ID binding in binding table
- If binding table entry exists, identify HA in binding; otherwise, pick HA (load balancing) and create temporary binding
416
RRQ(d=HAVA, s=FA, dest MAC=HA)
418
Standard Mobile IP processing (e.g., create tunnel interface and binding)
420
RRP(d=HAVA, s=HA, dest MAC = HACC)
422
Look up binding to obtain FA information from temporary binding; update binding with granted registration lifetime to create permanent binding
424
RRP(d=FA, s=HAVA)
426
RRP(d=MN, s=FA)

FIG. 4

502

Pending (temporary) bindings

MN ID (e.g., IP address) (NAI) 504	HAn (e.g., IP address) 506	FA address 508

FIG. 5A

510

Permanent bindings

MN ID (e.g., IP addr) (NAI) 512	HAn (e.g., IP addr) 514	Reg. lifetime 518	FA address 516

FIG. 5B

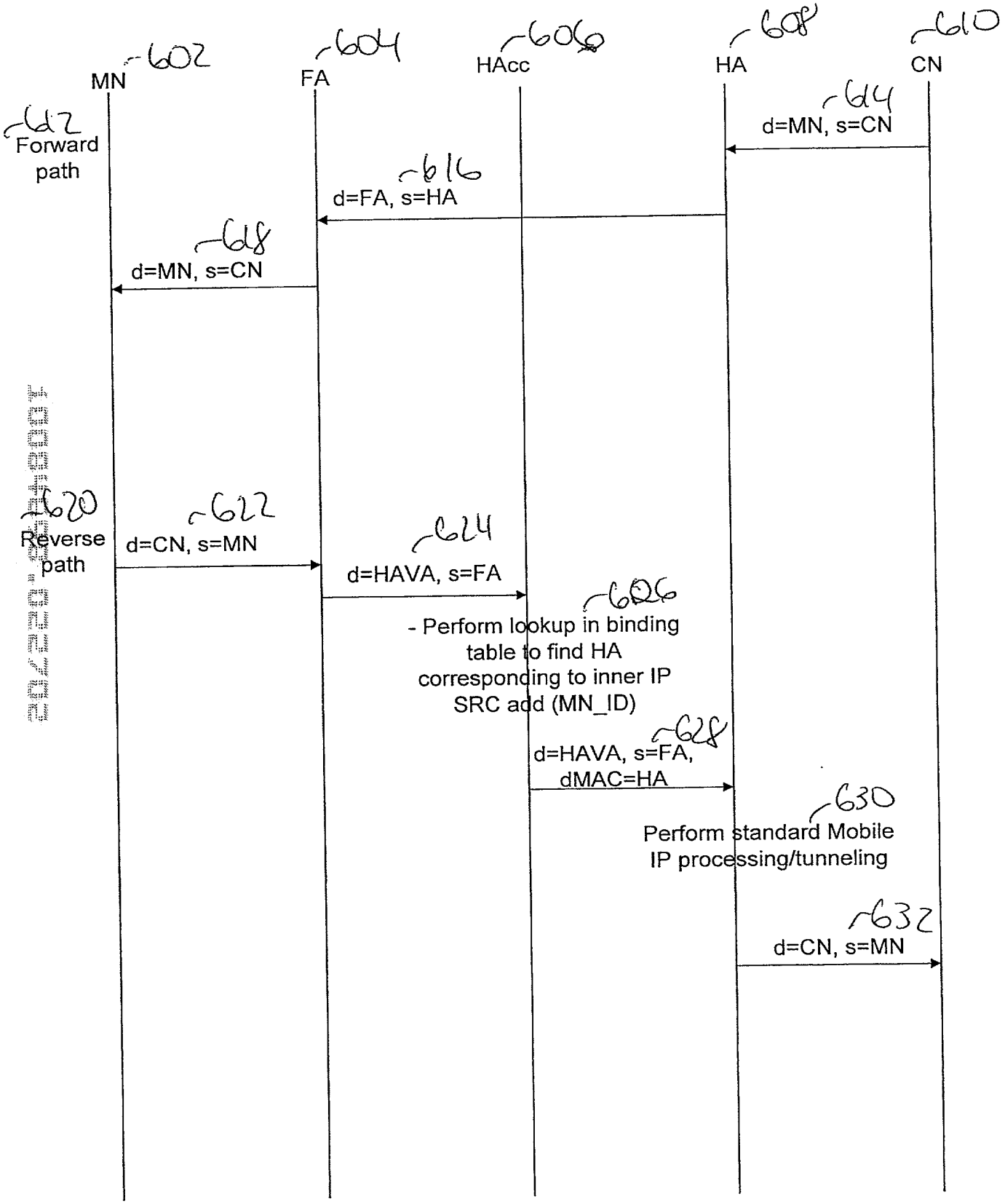

MN
602
FA
604
HAcc
606
HA
608
CN
610
612
Forward path
614
d=MN, s=CN
616
d=FA, s=HA
618
d=MN, s=CN
620
Reverse path
622
d=CN, s=MN
624
d=HAVA, s=FA
626
- Perform lookup in binding table to find HA corresponding to inner IP SRC add (MN_ID)
628
d=HAVA, s=FA, dMAC=HA
630
Perform standard Mobile IP processing/tunneling
632
d=CN, s=MN

FIG. 6

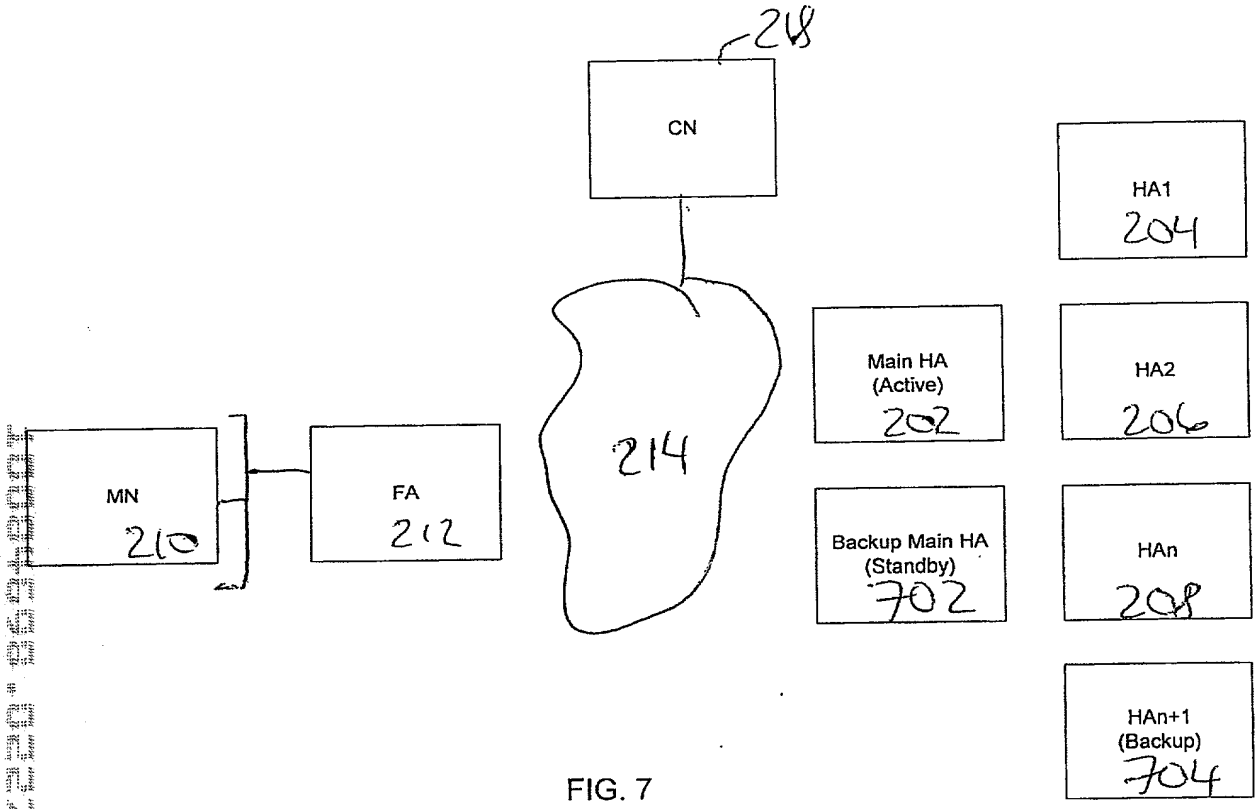

28
CN
214
MN
210
FA
212
Main HA
(Active)
202
Backup Main HA
(Standby)
702
HA1
204
HA2
206
HAn
208
HAn+1
(Backup)
704

FIG. 7

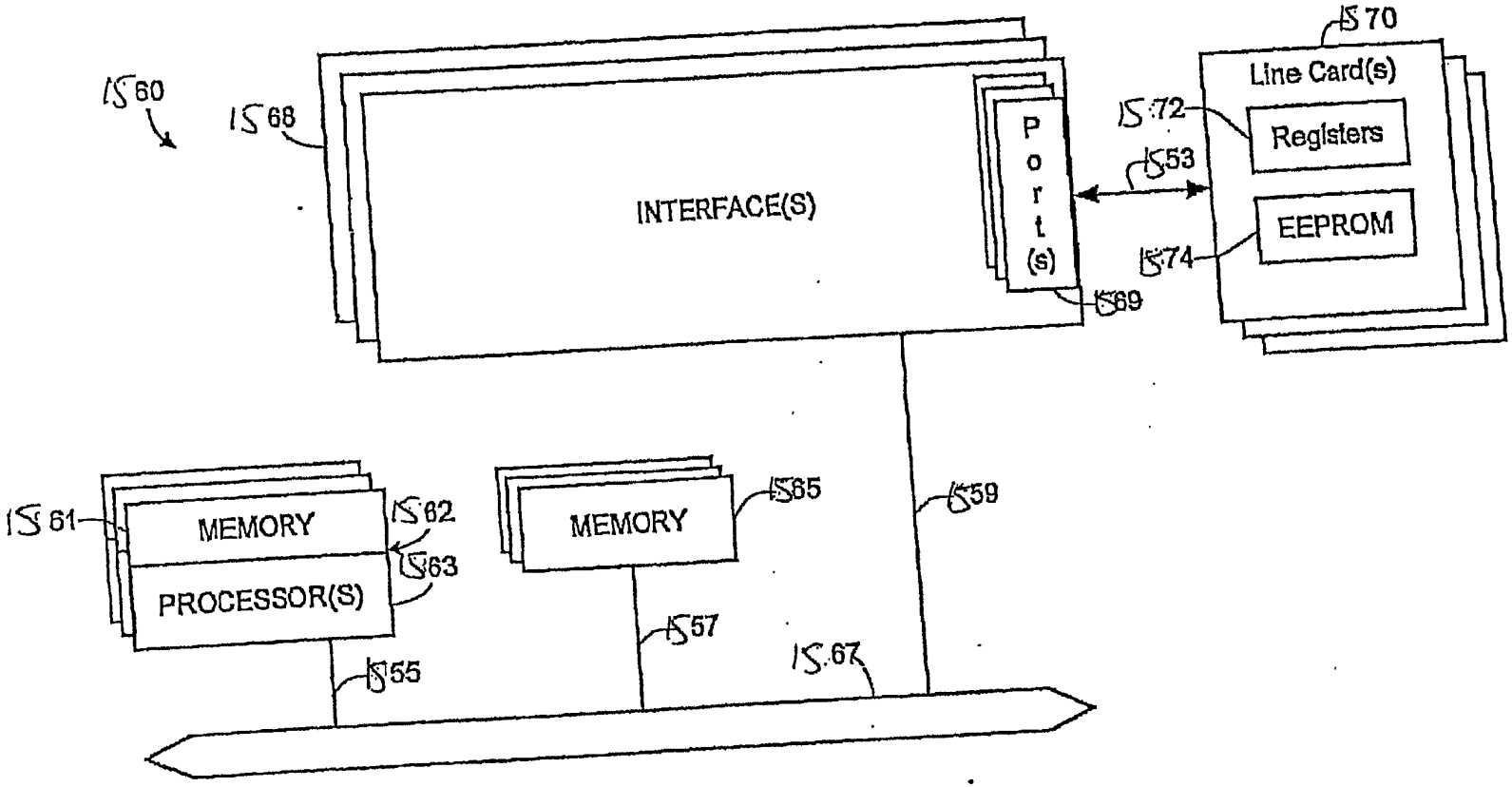

60
68
INTERFACE(S)
Port (s)
69
70
Line Card(s)
72
Registers
53
EEPROM
74
61
MEMORY
62
63
PROCESSOR(S)
55
MEMORY
65
57
59
67

Figure 8